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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Zahi Abuhamdeh,et al.

SERIAL NO.: 10/647,018 GROUP ART UNIT: 3732

FILED: August 22, 2003 EXAMINER:

FOR: Microprocessor Based Self-Diagnostic Port ATT'Y DOCKET: TRA-078

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

I hereby certify that this correspondence is being deposited on this day with the United States Postal Service as first class mail in an envelope addressed to : Commissioner of Patents and Trademarks, Washington, D.C. 20231.

David P. Gordon June 10, 2004
David P. Gordon Date
Reg. No. 29,996

Sir:

SUBMITTAL OF
DOCUMENTS PURSUANT TO DUTY OF DISCLOSURE

Pursuant to applicant's duty of disclosure 37 CFR Section 1.56, enclosed is a completed form PTOL-1449 which lists the documents relating to the above-referenced patent application. Since this document submittal is being presented prior to the first examination on the merits, no fee is due herewith.

Attached are the following articles:

"SCANSTA 101 Low Voltage IEEE 1149.1 STA Master", Specification Rev. DS101215, National Semiconductor Inc; 10/02 describes how it is designed to function as a test master for a IEEE 1149.1 test system. One of its features is to offload some of the processer overhead while remaining flexible.

"IEEE Std. 1149.1 (JTAG) TAP Masters with 8-Bit Generic Host Interfaces" Embedded Test-Bus Controllers; SCBS676D-December 1996-Revised 8/2002; describes its features and its architecture.

"IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices", ALTERA, September 2000, ver. 4.05; Application Note 39, describes the funtionality and efficiency of this system.

"A Brief Introduction to the JTAG Boundary Scan Interface", by Nick Patavalis, InAccess Networks, Athens, November 8, 2001; describes the general structure and interface signals.

The listed documents are brought to the Examiner's attention because they are known to the applicant and/or the applicant's attorney and may be considered by the Examiner to be material to his/her examination. This listing should not be construed as representation that a search has been made or that no better art exists. No inference should be made that the documents are in fact material merely because they are referenced herein. Moreover, no representation is made that the brief descriptions of the references herein necessarily describe the most material aspects of the references. Further, by this listing, the applicant is not making any admission regarding the relative dates of the invention and listed disclosures.

Respectfully submitted,

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INFORMATION DISCLOSURE CITATION

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Atty Docket No. TRA-078	Serial No. 10/647,018
Applicant Zahi Abuhamdeh et al.	
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		"SCANSTA 101 Low Voltage IEEE 1149.1 STA Master", Specification Rev. DS101215, National Semiconductor Inc.; October, 2002
		"IEEE Std. 1149.1 (JTAG) TAP Masters with 8-BIT Generic Host Interfaces" Embedded Test-Bus Controllers; SCBS676D-December 1996-Revised 8/2002
		"IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices", ALTERA September 2000, ver. 4.05 ; Application Note 39
		"A Brief Introduction to the JTAG Boundary Scan Interface", Nick Patavalis, Athens; November 8, 2001

EXAMINER	DATE CONSIDERED